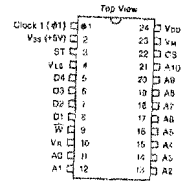
8192 Bit Electrically Alterable Read Only Memories

FEATURES

- 2048 x 4 Organization
- 11-Bit Binary Addressing
- Chip Select Input
- Electrically Reprogrammable
- 2.8 μs Access Time (ER2800)
- 1.65 μs Access Time (ER2805)
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



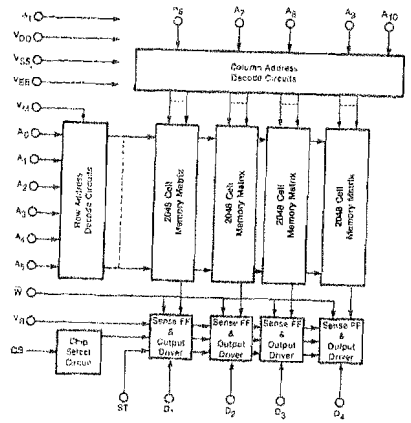
DESCRIPTION

The ER2800 and ER2805 are fully decoded 2048 × 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 2×10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}+28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^5 times. All outputs are at logic high when the device is in the erased state

BLOCK DIAGRAM


Column Address Decode Circuits
Row Address Decode Circuits
2048 Cell Memory Matrix
2048 Cell Memory Matrix
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2048 Cell Memory Matrix
Chip Select Circuit
Sense FF & Output Driver
Sense FF & Output Driver
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Sense FF & Output Driver

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS}	+0.3V to -30V
Operating ambient temperature	0°C to +70°C
Storage temperature	-65°C to +150°C
Soldering temperature of leads (10 seconds)	+300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}-0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{BB}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	--	V_{SS}	--	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	--	V_{SS}	--	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{LS}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{LS}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_W	Write control input low	V_{SS}-29	--	V_{SS}-4.4	V_{SS}-29	--	V_{SS}-4.4	Not Applicable			V
$V_{\phi 1}$	ϕ_1 input high voltage	--	V_{SS}	--	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V_{\phi L}$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{STH}	Strobe input high voltage	--	V_{SS}	--	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	--	V_{SS}-4.4	V_{DD}	--	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	--	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{LI}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1 = V_{DD} = V_{SS}$-20	--	--	-2.0	μA
$I_{\phi 1}$	ϕ_1 leakage current at V_{SS}-29V	$V_{DD} = V_{SS}$-29, ST=W=V_{SS}-25	--	--	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	--	--	-10.0	μA
I_{LLS}	Erase substrate leakage current at V_{SS}-28V	W=ST=V_{SS}-25	--	--	-200	μA
I_{DD_1}	V_{DD} supply current - read mode at V_{SS}-19V	ER2800	--	6.5	12	mA
		ER2805	--	11	13	mA
I_{DD_2}	V_{DD} supply current - V_{SS} = -28V	ER2800	--	18	25	mA
		ER2805	--	24	27	mA
I_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1KΩ, V_{CC}=V_{SS} (See TTL Notes)	V_{SS}-1.5	--	--	V
I_{OL}	Data output low voltage - TTL load		--	--	V_{SS}-6.6	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	--	--	V
V_{OL}	Data Output low voltage -- MOS	C_L=100 pF	--	--	V_{SS} -7	V
T_r	Unpowered nonvolatile data storage	Typical write conditions	10	--	--	Years

CAPACITANCE AT $V_{IN} = V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	--	5	7	pf
C_W	Write control input capacitance	--	10	20	pf
C_{ST}	Strobe input capacitance	--	10	15	pf
$C_{\phi 1}$	ϕ_1 Input Capacitance	--	40	50	pf
C_{LS}	Erase substrate capacitance	--	600	700	pf
C_D	Data input/output capacitance	--	6	10	pf

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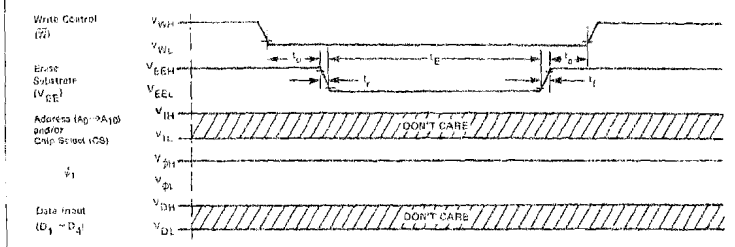
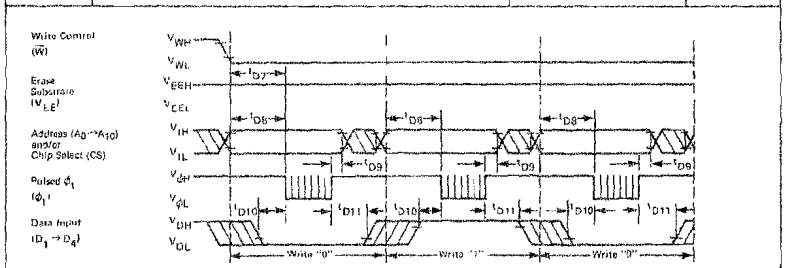
CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_c	Write-erase overlap	10	—	—	µs



WRITE CYCLE CHARACTERISTICS, T_A=0°C to +70°C ($\overline{ST}$=V_{DD}) (SEE NOTE 3)

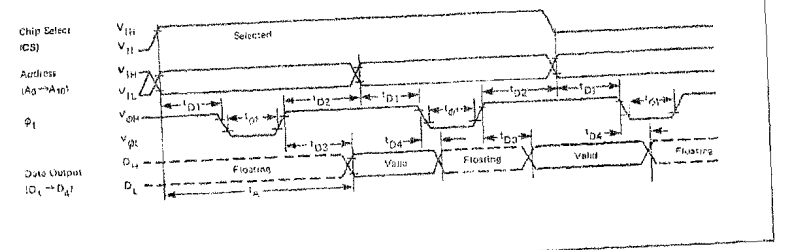
Symbol	Parameter	Min	Typ	Max	Units
$N_{\phi W}$	Number of ϕ_1 write pulses at 100 µs ±10%, 5 µs min. deadtime between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	µs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	µs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	µs
N_W	Number of times word may be rewritten	—	—	10[3]	—



NOTES
1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 µsec may result in a floated output condition. Consequently data must be resampled with a 40 µsec. time period following the fall of ϕ to ensure its validity
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected
4. All typical values are at +25°C and nominal voltages

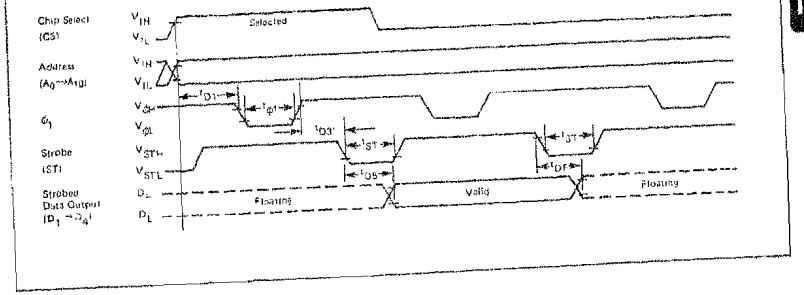
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, T_A=0°C to +70°C ($\overline{ST}$ = V_{DD})

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
T_A	Access time (strobe=V_{DD})	—	2.0	2.6	—	—	1.65	µs
$t_{\phi 1}$	Pulse width (rise and fall times ⩽50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
t_{D2}	ϕ_1 Fall to address and chip select change delay	0.0	—	—	0.0	—	—	µs
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)	—	—	950	—	—	550	ns
t_{D4}	ϕ_1 Rise to floated output delay	—	—	900	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION, T_A=0°C to +70°C

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ⩽ 50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
t_{D3}	ϕ_1 Fall to strobe rise delay	0.75	—	—	0.75	—	—	µs
t_{ST}	Strobe pulse width (rise and fall ⩽50 ns)	500	—	—	500	—	—	ns
t_{D5}	Strobe rise to strobed data output valid delay (See Notes 1 and 2)	—	—	950	—	—	500	ns
t_{DF}	Strobe rise to strobed floated output on deselect delay	—	—	300	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



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ER2800 TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C. R_S = 2K Ohms, V_{BS} = OV

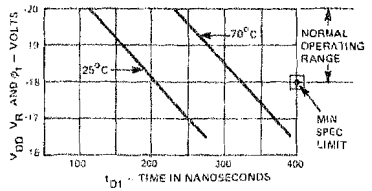


Fig. 1 TYPICAL ϕ1 DELAY IN NANOSECONDS vs. POWER SUPPLY VOLTAGE (ER2800)

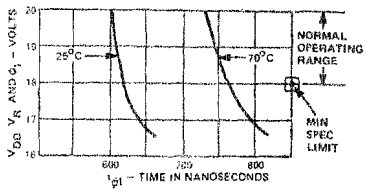


Fig. 2 TYPICAL ϕ1 WIDTH IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

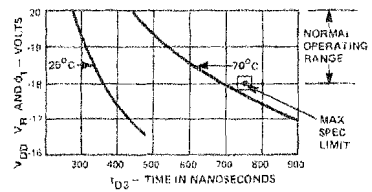


Fig. 3 TYPICAL DATA SETUP TIME IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

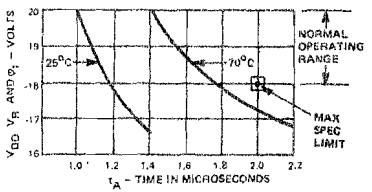


Fig. 4 TYPICAL ACCESS TIME IN MICROSECONDS vs. POWER SUPPLY IN VOLTAGES (ER2800)

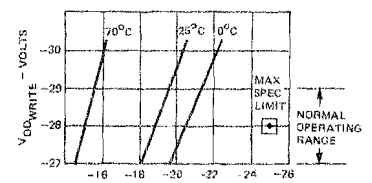


Fig. 5 TYPICAL WRITE CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGES (ER2800) (Deselected I_{DD2} = ¼ Graph I_{DD2})

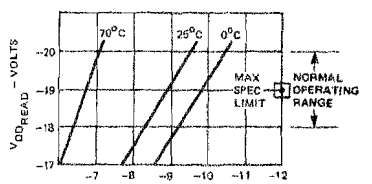


Fig. 6 TYPICAL READ CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGE (ER2800) (Chip selected or deselected)

PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or write data into the device

Data Input/Output (D1–D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition

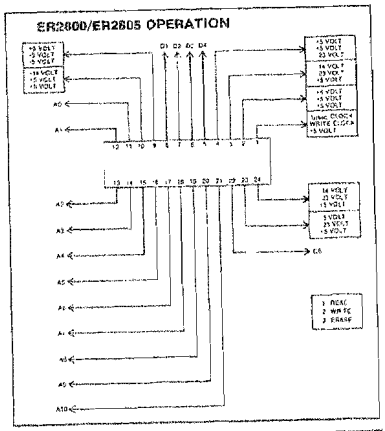
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device

Strobe (ST)
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle The ST input is high-level and not TTL-compatible

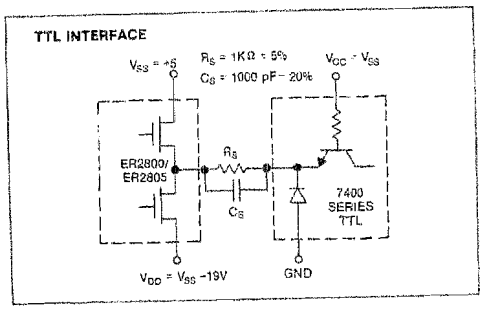
Phase One (ϕ1)
During the write operation, multiple 100µs pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltge to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible

NOTE All control, address and data inputs are TTL-compatible with pull-up resistors

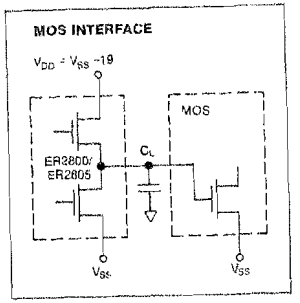
ER2800/ER2805 OPERATION



TTL INTERFACE



MOS INTERFACE



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